

**8M x 4Bit x 4 Banks Synchronous DRAM**

**FEATURES**

- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - . CAS Latency (2 & 3)
  - . Burst Length (1, 2, 4, 8)
  - . Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

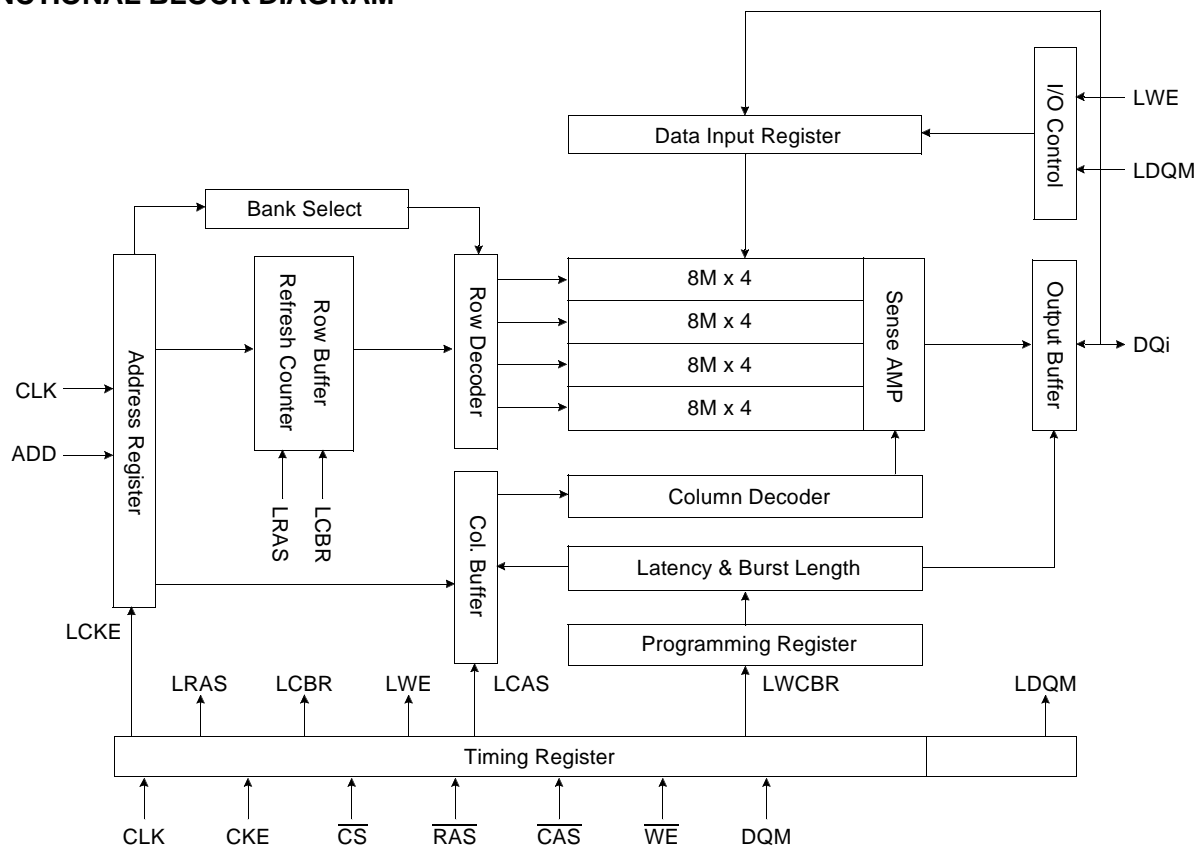
**GENERAL DESCRIPTION**

The KM44S32030 is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

**ORDERING INFORMATION**

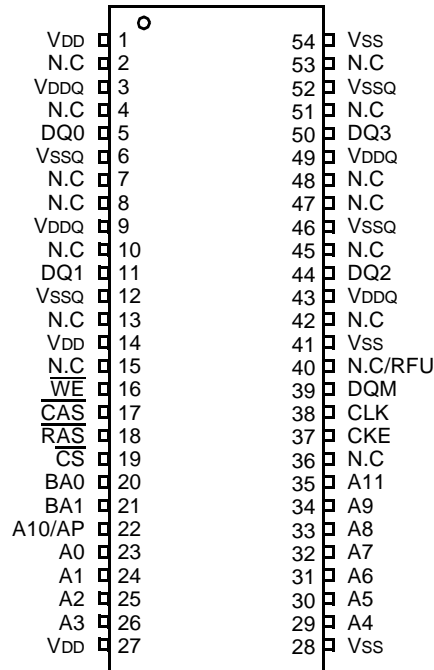
Part NO.	MAX Freq.	Interface	Package
KM44S32030T-G/F8	125MHz	LVTTTL	54pin TSOP(II)
KM44S32030T-G/FH	100MHz		
KM44S32030T-G/FL	100MHz		
KM44S32030T-G/F10	100MHz		

**FUNCTIONAL BLOCK DIAGRAM**



\* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)  
(400mil x 875mil)  
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA9, CA11
BA0 ~ BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from CAS, $\overline{WE}$ active.
DQM	Data Input/Output Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 3	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/ Reserved for Future Use	This pin is recommended to be left No Connection on the device.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	1	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS**

Recommended operating conditions (Voltage referenced to Vss = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	3.0	3.3	3.6	V	
Input logic high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input logic low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output logic high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output logic low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current(Inputs)	I <sub>IL</sub>	-5	-	5	uA	3
Input leakage current (I/O pins)	I <sub>IL</sub>	-5	-	5	uA	3,4

**Note :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>,  
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.  
4. Dout is disabled, 0V ≤ V<sub>OUT</sub> ≤ V<sub>DDQ</sub>.

**CAPACITANCE** (V<sub>DD</sub> = 3.3V, TA = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Clock	C <sub>CLK</sub>	2.5	4	pF
$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{CS}}$ , CKE, DQM	C <sub>IN</sub>	2.5	5	pF
Address	C <sub>ADD</sub>	2.5	5	pF
DQ <sub>0</sub> ~ DQ <sub>3</sub>	C <sub>OUT</sub>	4	6.5	pF

**DC CHARACTERISTICS**

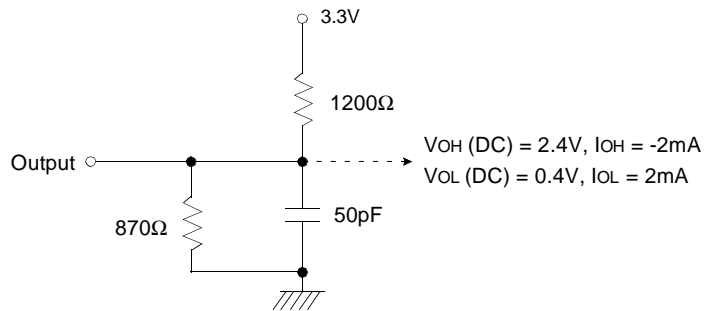
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version				Unit	Note
				-8	-H	-L	-10		
Operating Current (One Bank Active)	ICC1	Burst Length =1 trc ≥ trc(min) IOL = 0 mA		120	110	110	105	mA	1
Precharge Standby Current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		1				mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Precharge Standby Current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tcc=15ns Input signals are changed one time during 30ns		15				mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		7					
Active Standby Current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		5				mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		5					
Active Standby Current in non power-down mode (One Bank Active)	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tcc = 15ns Input signals are changed one time during 30ns.		30				mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20					
Operating Current (Burst Mode)	ICC4	IOL = 0 mA Page Burst tCCD = 2CLKs	3	140	115	115	115	mA	1
			2	105	115	105	105		
Refresh Current	ICC5	trc ≥ trc(min)		200			165	mA	2
Self Refresh Current	ICC6	CKE ≤ 0.2V		1				mA	3
				600				uA	4

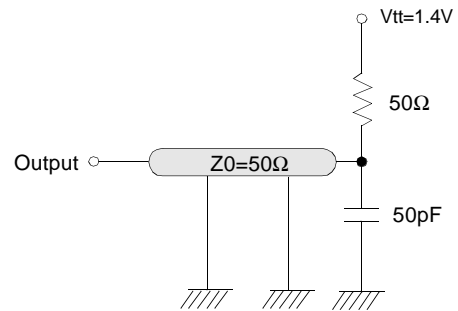
- Note :**
1. Measured with outputs open.
  2. Refresh period is 64ms.
  3. KM44S32030T-G\*\*
  4. KM44S32030T-F\*\*

**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^\circ C$ )

Parameter	Value	Unit
Input levels ( $V_{ih}/V_{il}$ )	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r / t_f = 1 / 1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version				Unit	Note
		-8	-H	-L	-10		
Row active to row active delay	$t_{RRD}(\min)$	16	20	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	20	20	20	24	ns	1
Row precharge time	$t_{RP}(\min)$	20	20	20	24	ns	1
Row active time	$t_{RAS}(\min)$	48	50	50	50	ns	1
	$t_{RAS}(\max)$	100				us	
Row cycle time	$t_{RC}(\min)$	68	70	70	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	8	10	10	12	ns	2
Last data in to new col. address delay	$t_{CDL}(\min)$	1				CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1				CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1				CLK	3
Number of valid output data	CAS latency=3	2				ea	4
	CAS latency=2	1					

- Note :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.

**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)

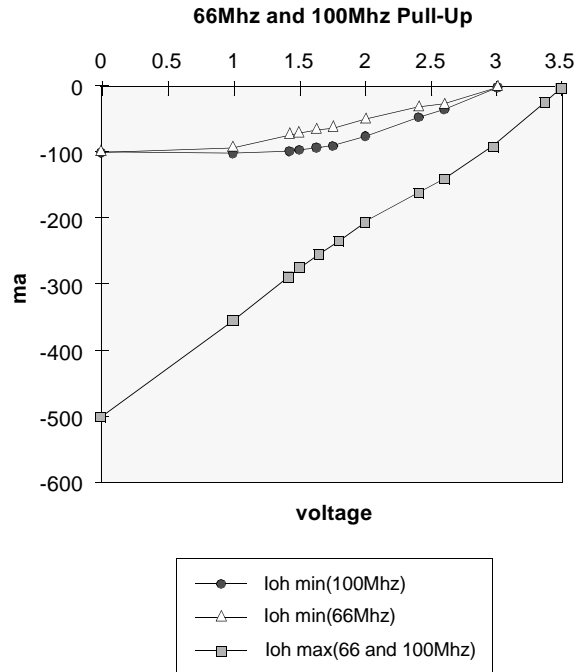
Parameter		Symbol	-8		-H		-L		-10		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	8	1000	10	1000	10	1000	10	1000	ns	1
	CAS latency=2		12		10		12		13			
CLK to valid output delay	CAS latency=3	tsac		6		6		6		7	ns	1, 2
	CAS latency=2			6		6		7		7		
Output data hold time	CAS latency=3	toH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tch	3		3		3		3.5		ns	3
CLK low pulse width		tcl	3		3		3		3.5		ns	3
Input setup time		tss	2		2		2		2.5		ns	3
Input hold time		tsh	1		1		1		1.5		ns	3
CLK to output in Low-Z		tslz	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tshz		6		6		6		7	ns	
	CAS latency=2			6		6		7		7		

- Note :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
  - Assumed input rise and fall time (tr & tf)=1ns.  
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.

**IBIS Specification**

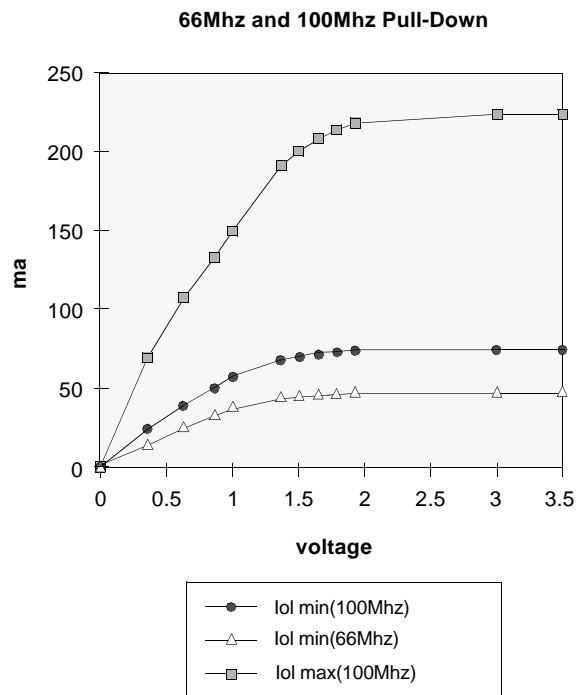
**IOH Characteristics(Pull-up)**

Voltage	100Mhz min	100Mhz max	66Mhz min
(V)	I(mA)	I(mA)	I(mA)
3.45		-2.4	
3.3		-27.3	
3	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2	-58.7	-197	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73	-248	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1	-88.6	-344.5	-72.5
0	-93	-502.4	-93



**IOI Characteristics(Pull-Down)**

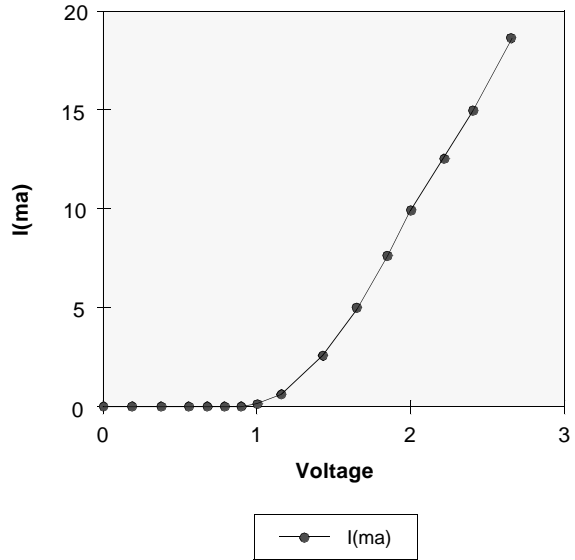
Voltage	100Mhz min	100Mhz max	66Mhz min
(V)	I(mA)	I(mA)	I(mA)
0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3	80.3	219.6	54.2
3.45	81.4	222.6	54.9



Vdd Clamp @CLK,CKE,  $\overline{CS}$ ,DQM & DQ

VDD	I(mA)
0.0V	0.0mA
0.2V	0.0mA
0.4V	0.0mA
0.6V	0.0mA
0.7V	0.0mA
0.8V	0.0mA
0.9V	0.0mA
1.0V	0.23mA
1.2V	1.34mA
1.4V	3.02mA
1.6V	5.06mA
1.8V	7.35mA
2.0V	9.83mA
2.2V	12.48mA
2.4V	15.30mA
2.6V	18.31mA

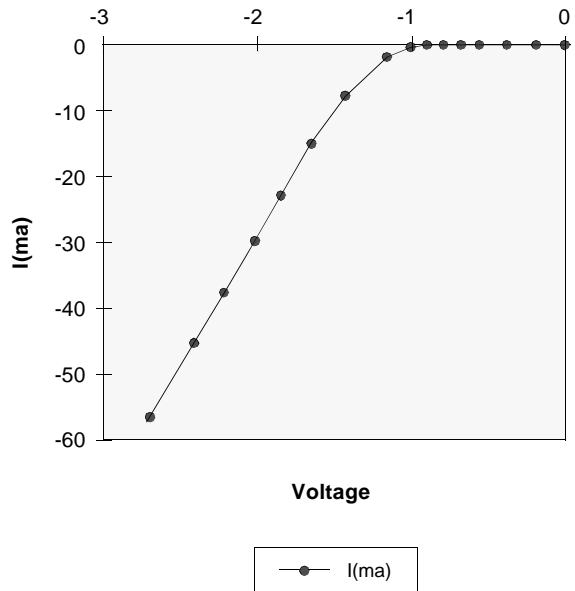
Minimum VDD Clamp Current  
(referenced to VDD)



Vss Clamp @CLK,CKE,  $\overline{CS}$ ,DQM & DQ

VSS	I(mA)
-2.6	-57.23mA
-2.4	-45.77mA
-2.2	-38.26mA
-2.0	-31.22mA
-1.8	-24.58mA
-1.6	-18.37mA
-1.4	-12.56mA
-1.2	-7.57mA
-1.0	-3.37mA
-0.9	-1.75mA
-0.8	-0.58mA
-0.7	-0.05mA
-0.6	0.0mA
-0.4	0.0mA
-0.2	0.0mA
0.0	0.0mA

Minimum VSS Clamp Current





# KM44S32030

# Preliminary CMOS SDRAM

## FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

### KM44S32030T-8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		68ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

### KM44S32030T-H

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (10.0ns)	2	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

### KM44S32030T-L

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

### KM44S32030T-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	12ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	2
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note	
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			1, 2	
Refresh	Auto Refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self Refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.		H	X	L	L	H	H	X	V	Row Address			
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	X	V	L	Column Address (A0~A9,A11)	4	
	Auto Precharge Enable									H		4, 5	
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	X	V	L	Column Address (A0~A9,A11)	4	
	Auto Precharge Enable									H		4, 5	
Burst Stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank Selection	H	X	L	L	H	L	X	V	L	X		
	All Banks								X	H			
Clock Suspend or Active Power Down	Entry	H	L	H	X	X	X	X	X				
				L	V	V	V						
	Exit	L	H	X	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	L	H	H	X	X	X	X	X				
				L	V	V	V						
DQM		H	X					V	X		7		
No Operation Command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

**Note :** 1. OP Code : Operand Code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)